REMARKS

In response to the final Official Action of June 29, 2007, minor amendments have been made to claim 24, line 9, and claim 42, line 8 to correct grammatical errors. No new matter has been introduced.

Section 1 of the office action acknowledges that there are 23 claims pending in the application, all of which are ready for examination by the Examiner.

Section 2 of the office action acknowledges that the request for continued examination filed after final rejection was received and corresponding fees paid in a timely manner. The submission has been entered by the Office.

Section 3 of the office action acknowledges that the amendments made to the specification in the above submission have been entered by the Office.

35 U.S.C. 103(a) Rejections

At section 4 of the office action, the Office rejects claims 24, 28-43 and 45 under 35 U.S.C. 103(a) as being unpatentable over *Camacho et al.* (U.S. 6,167,487, hereafter referred to as *Camacho*) in view of *Ware et al.* (U.S. 6,826,657, hereafter referred to as *Ware*). For the reasons set forth below, the Applicant respectfully requests reconsideration of the rejection.

In the office action, the Office correctly asserts that *Camacho* does not disclose expressively the case of sole addressing in which the data is provided through data ports of both terminals. However, the Office is of the opinion that *Ware* discloses this feature. In particular, the Office cites col. 15 as well as Figs. 6a and 6b of *Ware* as indicating the feature of sole addressing according to the invention. Applicant respectfully disagrees.

More particularly, at section 6 of the office action, the Office rejects independent claims 24, 41-42 and 45 as unpatentable over *Camacho* in view of *Ware*. According to current claims 24, 41-42 and 45, in the case of sole addressing, "the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provide the data through data ports of both terminals." According to the claims, in the case of sole addressing, address and control ports of only one of the terminals are used. When using only address and control ports of one of the terminals, in order to increase the data bandwidth, the claimed invention teaches that data is provided through data ports of both terminals. This feature provides that even when accessing the data through address and control ports via only one terminal, the data bandwidth is increased by using the data ports of both terminals. The teaching of *Ware* differs completely.

According to *Ware*, col. 15, lines 14-24, "in a first mode, some of the storage locations in the memory component are accessible through the QDx data bus... and the remaining storage locations in the memory component are accessible through the QDy data bus". This is the case of individual addressing in the present invention, where data is accessed and addressed through each of the terminals, respectively. In the second mode, according to *Ware*, "all the storage locations in the memory component are accessible through the QDx data bus, and the QDy data bus is unused" (emphasis added). It is understood that, when the QDy data bus is unused, the data ports of the QDy data terminal are not used. Thus, the memory controllers do not provide the data through data ports of both terminals, but rather through data ports of only the QDx data bus, and the data ports of the QDy data bus are unused. This is completely different to the teaching of the present invention, where the data ports of both terminals are used for providing the data in the case of sole addressing.

This teaching is further repeated at *Ware* col. 15, line 45, and col. 16, lines 3, 12-13. *Ware* teaches accessing the whole memory through only one data port, namely the QDx data bus. While accessing the data through only the QDx data bus, the QDy data bus is unused, thus it is impossible that the QDy data ports are used for accessing the data, as is taught by the claimed invention. Thus, *Camacho* in view of *Ware* does not

disclose the limitation of the claimed invention that in the case of sole addressing, "the access controllers provide access to the memory areas by control ports and address ports of only one of the terminals and provide the data through data ports of both terminals." Therefore, *Camacho* in view of *Ware* does not render claims 24, 41-42 and 45 obvious.

At section 7 of the office action, the Office rejects claim 28 as being unpatentable over *Camacho* in view of *Ware*. Claim 28 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 28 obvious.

At section 8 of the office action, the Office rejects claim 29 as being unpatentable over *Camacho* in view of *Ware*. Claim 29 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 29 obvious.

At section 9 of the office action, the Office rejects claim 30 as being unpatentable over *Camacho* in view of *Ware*. Claim 30 is dependent from claim 29, which in turn is dependent from claim 24, and recites features not recited in claims 29 or 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 30 obvious.

At section 10 of the office action, the Office rejects claim 31 as being unpatentable over *Camacho* in view of *Ware*. Claim 31 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 31 obvious.

At section 11 of the office action, the Office rejects claims 32-33 as being unpatentable over *Camacho* in view of *Ware*. Claims 32-33 are dependent from claim

24 and recite features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claims 32-33 obvious.

At section 12 of the office action, the Office rejects claim 34 as being unpatentable over *Camacho* in view of *Ware*. Claim 34 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 34 obvious.

At section 13 of the office action, the Office rejects claims 35-36 as being unpatentable over *Camacho* in view of *Ware*. Claims 35-36 are dependent from claim 24 and recite features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claims 35-36 obvious.

At section 14 of the office action, the Office rejects claim 37 as being unpatentable over *Camacho* in view of *Ware*. Claim 37 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 37 obvious.

At section 15 of the office action, the Office rejects claim 38 as being unpatentable over *Camacho* in view of *Ware*. The Office is of the opinion that providing an independent burst length counter, burst termination logic and memory addressing logic for burst mode operations for port A independently of burst mode operations for port B, (*Ware* col. 8, lines 27,31) would disclose programming the size of the memory areas through one of the terminals. The size of a memory area is independent of the burst length of accessing the memory. The burst length defines how many clock pulses are used to address one memory area. The longer a burst, the wider the address range which is addressable. However, the size of the memory area is different and independent of a burst length definition. Therefore, *Ware* does not anticipate programming the size of the memory areas through one of the terminals. Furthermore, Claim 38 is dependent from claim 24 and recites features not recited in claim 24. For

the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 38 obvious.

At section 16 of the office action, the Office rejects claim 39 as being unpatentable over *Camacho* in view of *Ware*. Claim 39 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 39 obvious.

At section 17 of the office action, the Office rejects claim 40 as being unpatentable over *Camacho* in view of *Ware*. According to claim 40, the bandwidth and clocking frequency may be different for each of the terminals. The Office is of the opinion that programming ports A and B individually, so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data bus of another length (*Ware* col. 7, line 57- col. 8, line 31), would disclose different bandwidths and clocking frequencies at the terminals. However, the bandwidth and the clocking frequency are different parameters than the burst length. Burst length, as explained above, is a size of an addressing sequence. The longer the burst, the wider the address space which is addressable. However, increasing the burst length does not influence bandwidth or clocking frequency. Therefore, providing different data burst length at the different ports, according to *Ware*, does not anticipate providing different bandwidth and clocking frequency at the terminals, as set forth in claim 40. Furthermore, claim 40 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 40 obvious.

At section 18 of the office action, the Office rejects claim 43 as being unpatentable over *Camacho* in view of *Ware*. Claim 43 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 43 obvious.

At section 19 of the office action, the Office rejects claim 25 as being unpatentable over *Camacho* in view of *Ware*. According to *Ware*, Fig. 13c and related text, a memory controller with three ports 214, 216, 242 is disclosed. Port 214 is connected to memory controller 212 via the QDx data bus. The QDy data bus of first memory module 218 is connected to the QDx data bus of the second memory module 232. The QDy data bus of the second memory module 232 is connected to the QDx data bus of the third memory module 244. The QDy data bus of the third memory module 244 is connected to the third port 242 of the memory controller 212. The second memory module is only connected indirectly to memory controller 212 through a connection between the QDx data bus of the second memory module 232, and the QDy data bus of the first memory module 218, and through a connection between the QDy data bus of the second memory module 232 and the QDx data bus of the third memory module 244. According to current claim 25, however, a third memory area provides access by the control ports and address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals respectively. That is, the third memory module needs to be accessible by both controllers. Considering port 214 as a first controller and port 242 as a second controller, according to *Ware*, the first controller is connected to first memory area 218, and the second memory controller 242 is connected to the second memory area 244. However, control and address ports as well as data ports of both terminals are not connected to the third memory module 232, and therefore are not providing access by the control and address ports of both terminals. Consequently, claim 25 is not anticipated by *Camacho* in view of *Ware*. Furthermore, claim 25 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 25 obvious.

At section 20 of the office action, the Office rejects claim 26 as being unpatentable over *Camacho* in view of *Ware*. Claim 26 is dependent from claim 25, which in turn is dependent from claim 24, and recites features not recited in claims 25 or

24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 26 obvious.

At section 21 of the office action, the Office rejects claim 27 as being unpatentable over *Camacho* in view of *Ware*. Claim 27 is dependent from claim 25, which in turn is dependent from claim 24, and recites features not recited in claims 25 or 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 27 obvious.

At section 22 of the office action, the Office rejects claim 46 as being unpatentable over *Camacho* in view of *Ware*. Claim 46 is dependent from claim 45, which is a means-plus-function claim reciting the same limitation as claim 24 (namely "wherein in case of sole addressing and accessing the data, said means for selectively providing access to the first and second means for storing data is by control ports and address ports of only one of the first and second means for accessing data and provides the data through data ports of both the first and second means for accessing data") and recites features not recited in claims 45 or 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 46 obvious.

At section 23 of the office action, the Office rejects claim 44 as being unpatentable over *Camacho* in view of *Ware*. Claim 44 is dependent from claim 24 and recites features not recited in claim 24. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render claim 44 obvious.

At section 24 of the office action, the Office further asserts that the combination of *Camacho* in view of *Ware* does not disclose a mobile communication device comprising a memory unit according to claim 24, but that it would have been obvious to one of ordinary skill in the art at the time of the invention to use the memory as being claimed in claim 24 in a mobile communication device. For the reasons regarding claim 24 above, *Camacho* in view of *Ware* does not render the claimed invention obvious.

CONCLUSION

In view of the preceding arguments, independent claims 24, 41-42 and 45 are non-obvious over *Camacho* in view of *Ware* and are believed to be allowable. Claims 26-40, 43-44 and 46 are dependent claims and recite features not recited in the independent claims. For the reasons regarding claims 24, 41-42 and 45 above, *Camacho* in view of *Ware* does not render the claimed invention obvious. Therefore, all of the dependent claims are further distinguished over the cited art. In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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Cathy A. Sturmer
Agent for Applicants
Registration No. 60,869

WARE, FRESSOLA, VAN DER
SLUYS & ADOLPHSON LLP
Building Five, Bradford Green
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955